AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning at line 8 of page 22 with the following amended paragraph:

Referring back to Figure 6 again, wherein an embodiment of processor interface 112 of Fig. 3 is illustrated. As illustrated, for the embodiment, for the ingress packet side, processor interface 112 includes a number of ingress data read and write (R/W) registers, and their associated processor control slave logic 156, ingress diverted packet unpacker and data formatter [[158]] 160, and ingress insert data packer and SOP/EOP generation logic [[160]] 158.

Please replace the paragraph beginning at line 14 of page 22 with the following amended paragraph:

Ingress data R/W registers, and their associated processor control slave logic 156 are employed to facilitate a host processor in retrieving the ingress diverted packet data and providing the ingress insert packet data. In response to a notice of the ingress diverted packet data being ready for a host processor to retrieve, the host processor generates the appropriate control signal for ingress diverted packet unpacker and data formatter [[158]] 160 through the associated processor control slave logic 156. Ingress diverted packet unpacker and data formatter [[158]] 160 in response, generates the appropriate read enable signals for the ingress diverted packet storage structure 122b. Further, unpacker and data formatter 172 reads the gap-compressed packet data and the associated SOP, EOP and bad packet indicator from storage structure 122b, and "unpack" them for placement onto the appropriate bit

positions of the data bus. The process continues until the EOP is encountered (i.e. the applicable EOP bit set).

Please replace the paragraph beginning at line 1 of page 23 with the following amended paragraph:

In like manner, a host processor generates the appropriate control signal for ingress insert data packer and SOP/EOP generation [[160]] 158 through the associated processor control slave logic 156. Ingress insert data packer and SOP/EOP generation [[160]] 158 in response, generates the appropriate write enable signals for the ingress insert storage structure 122c. Further, data packer and SOP/EOP generation [[160]] 158 writes the Insert data and the associated SOP, EOP and bad packet indicator bits into storage structure 122c in "packed" form, and the unpacked portions are successively taken off the appropriate bit positions of the data bus.